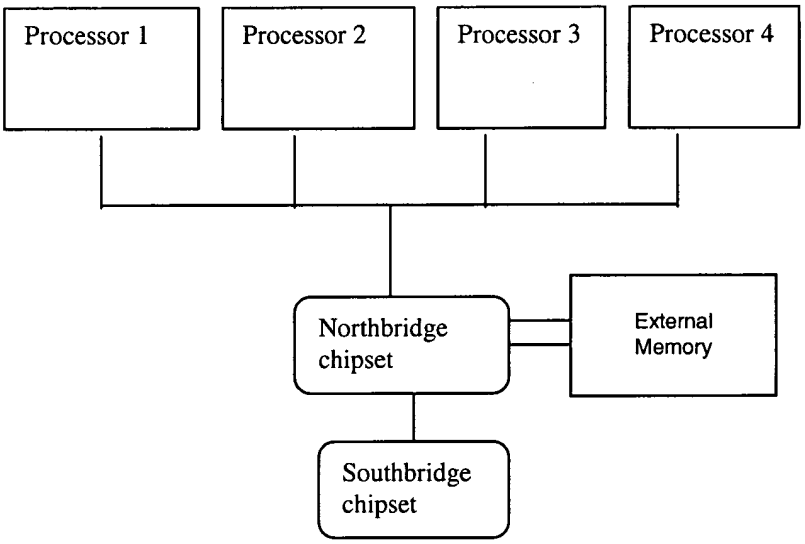
Processor 1
Processor 2
Processor 3
Processor 4
Northbridge chipset
External Memory
Southbridge chipset

Figure 1

200

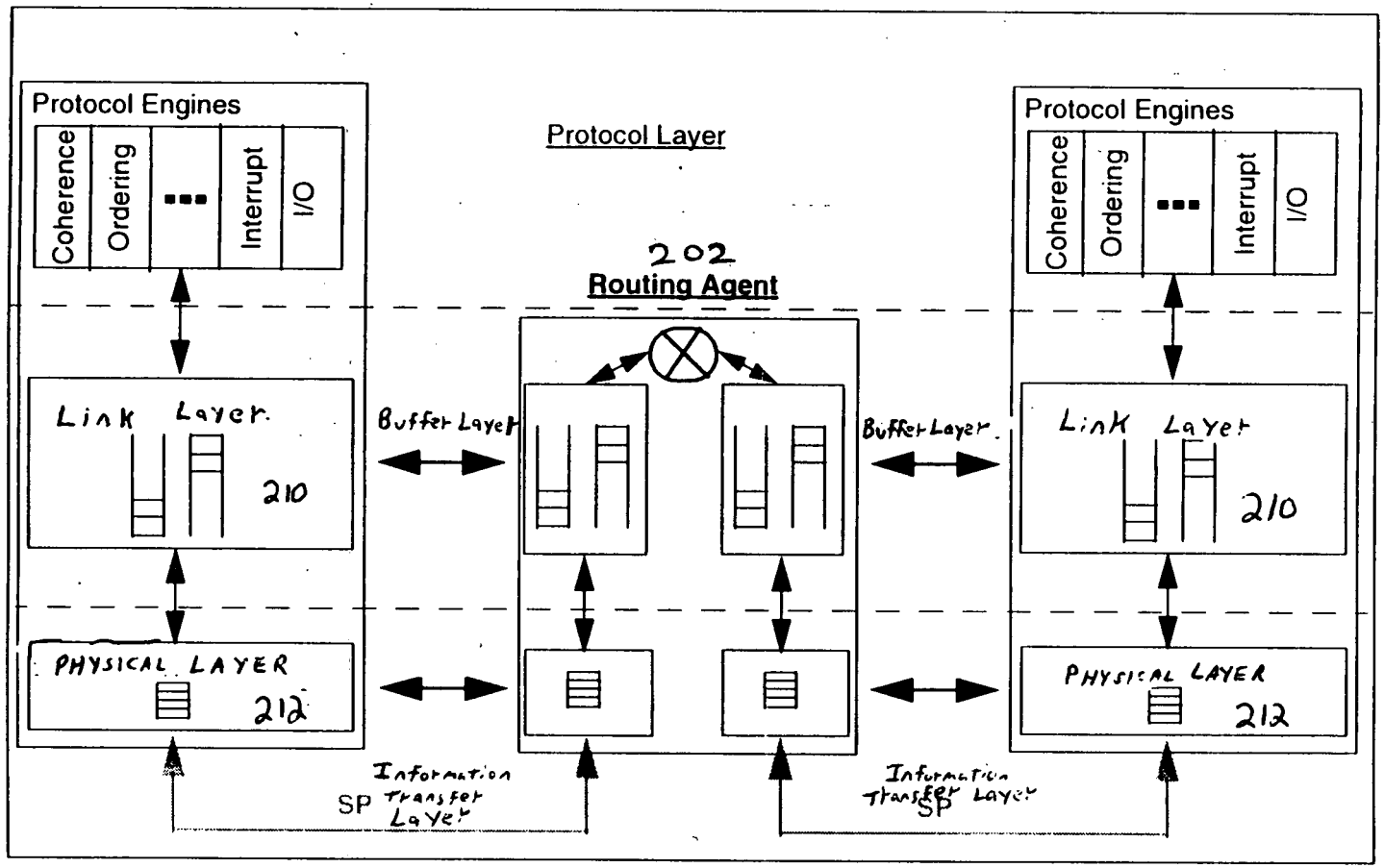

Figure 2

300

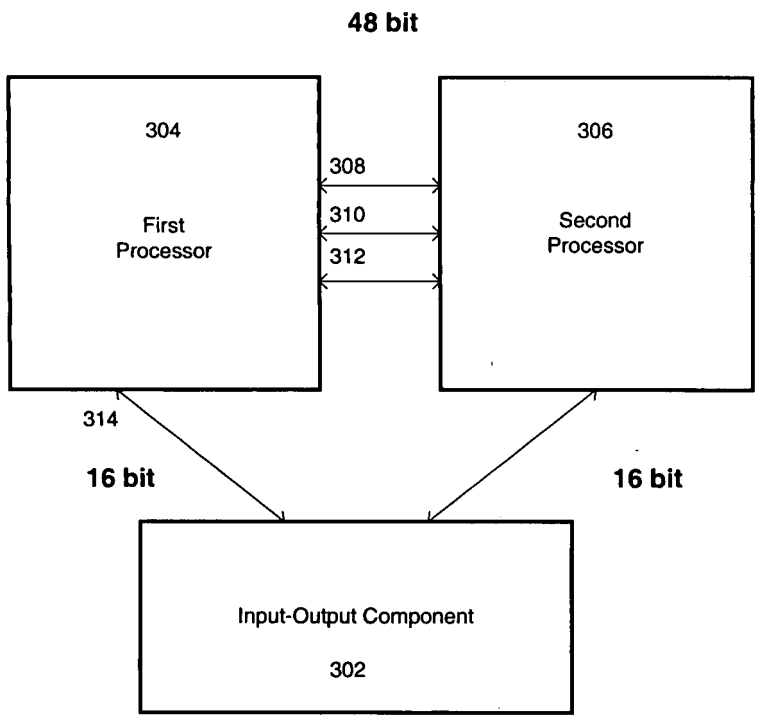

Figure 3

400

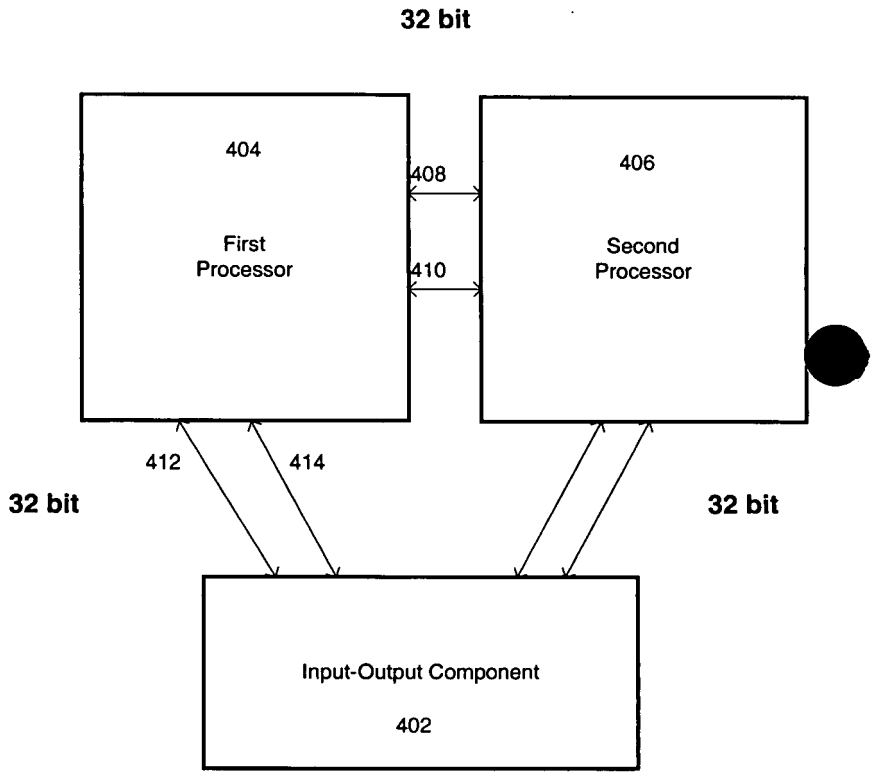

Figure 4

500

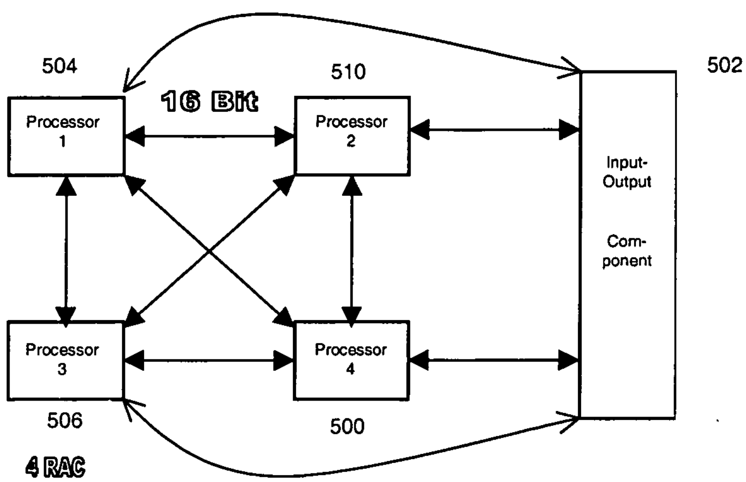
504
510
502
16 Bit
Processor 1
Processor 2
Input-Output Com-ponent
Processor 3
Processor 4
506
500
4 RAC

Figure 5

600

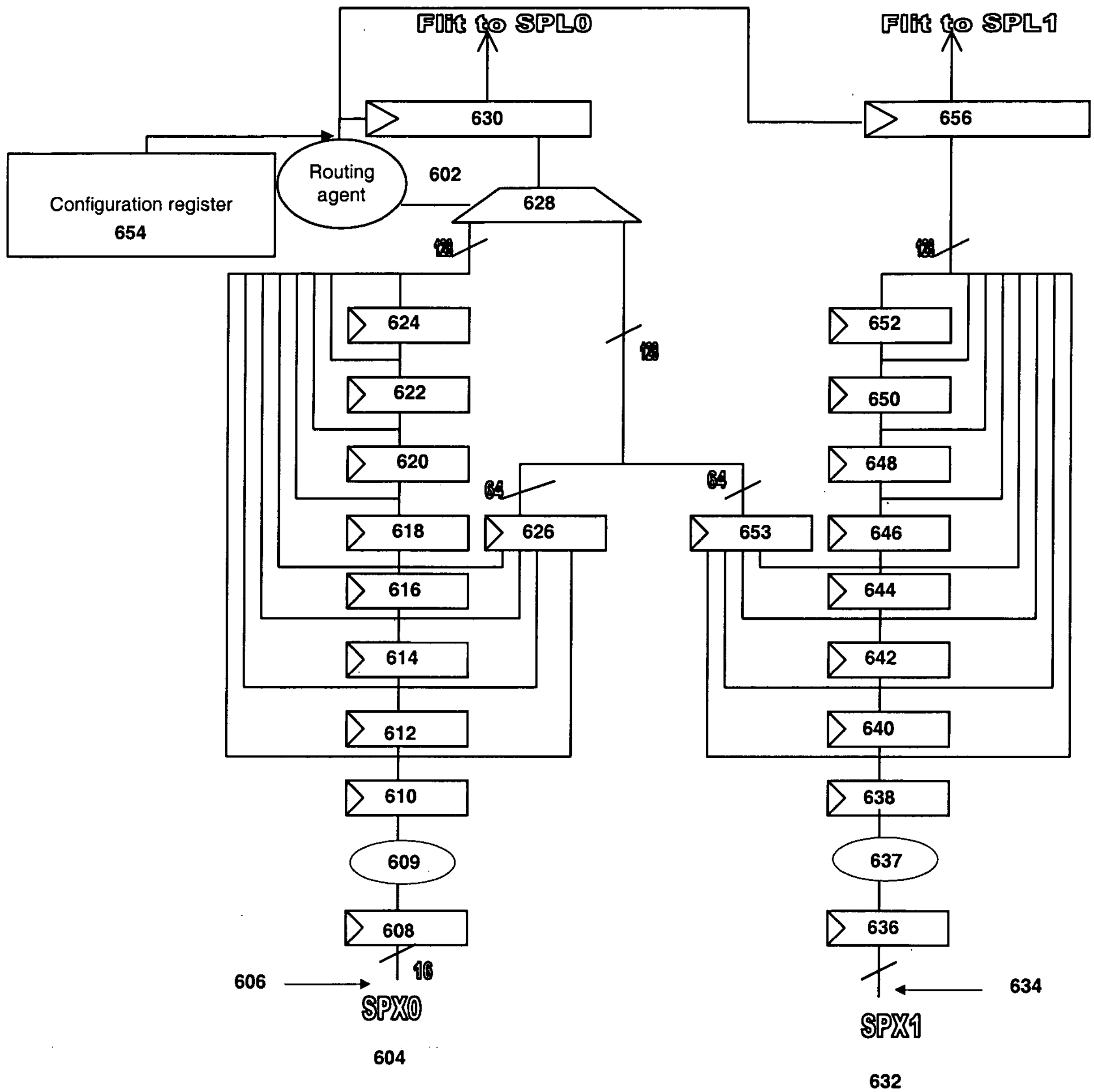

Figure 6

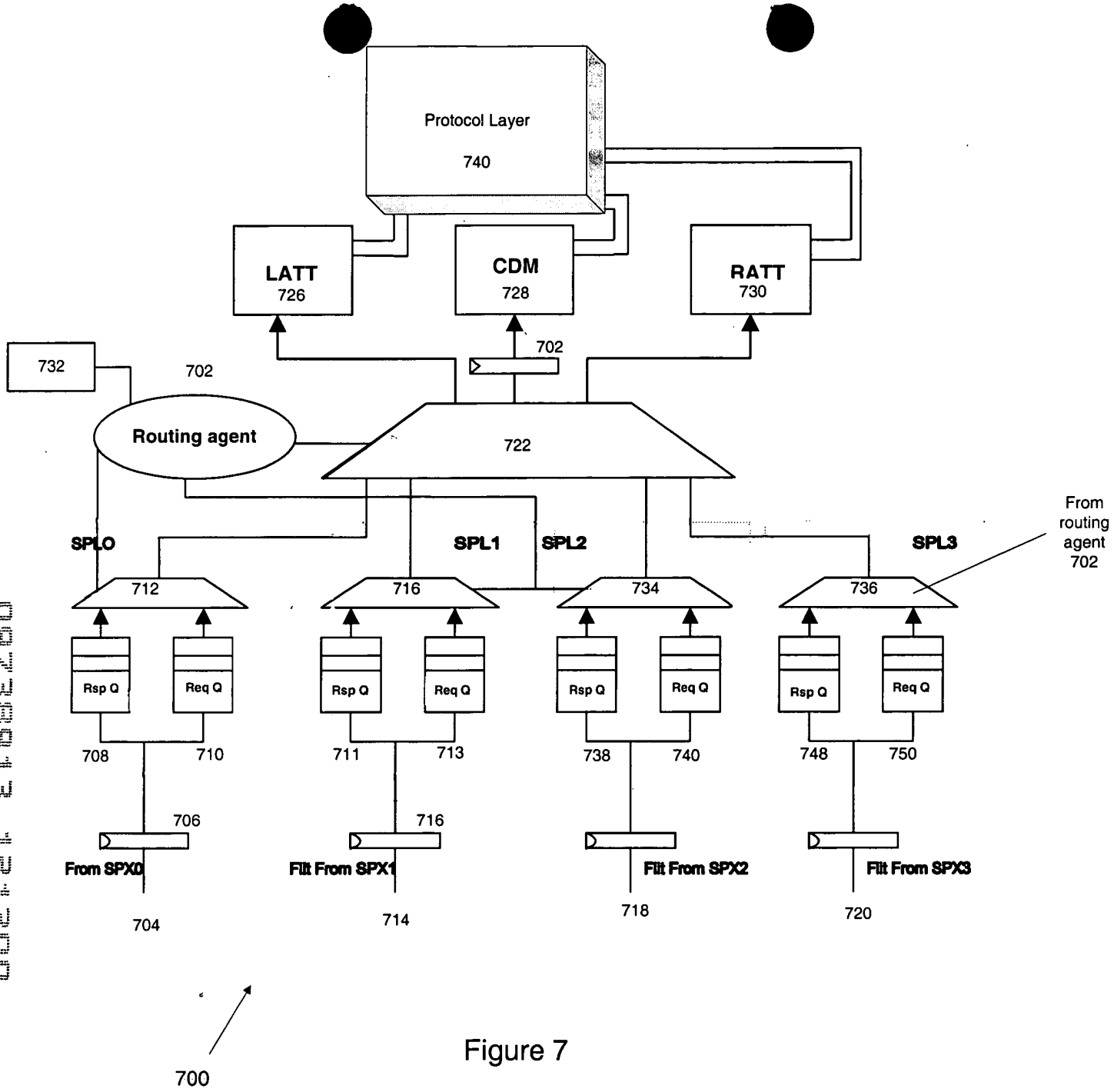
Protocol Layer
740
LATT
726
CDM
728
RATT
730
732
702
702
Routing agent
722
From routing agent 702
SPL0
SPL1
SPL2
SPL3
712
716
734
736
Rsp Q
Req Q
Rsp Q
Req Q
Rsp Q
Req Q
Rsp Q
Req Q
708
710
711
713
738
740
748
750
706
716
From SPX0
Flit From SPX1
Flit From SPX2
Flit From SPX3
704
714
718
720
700

Figure 7

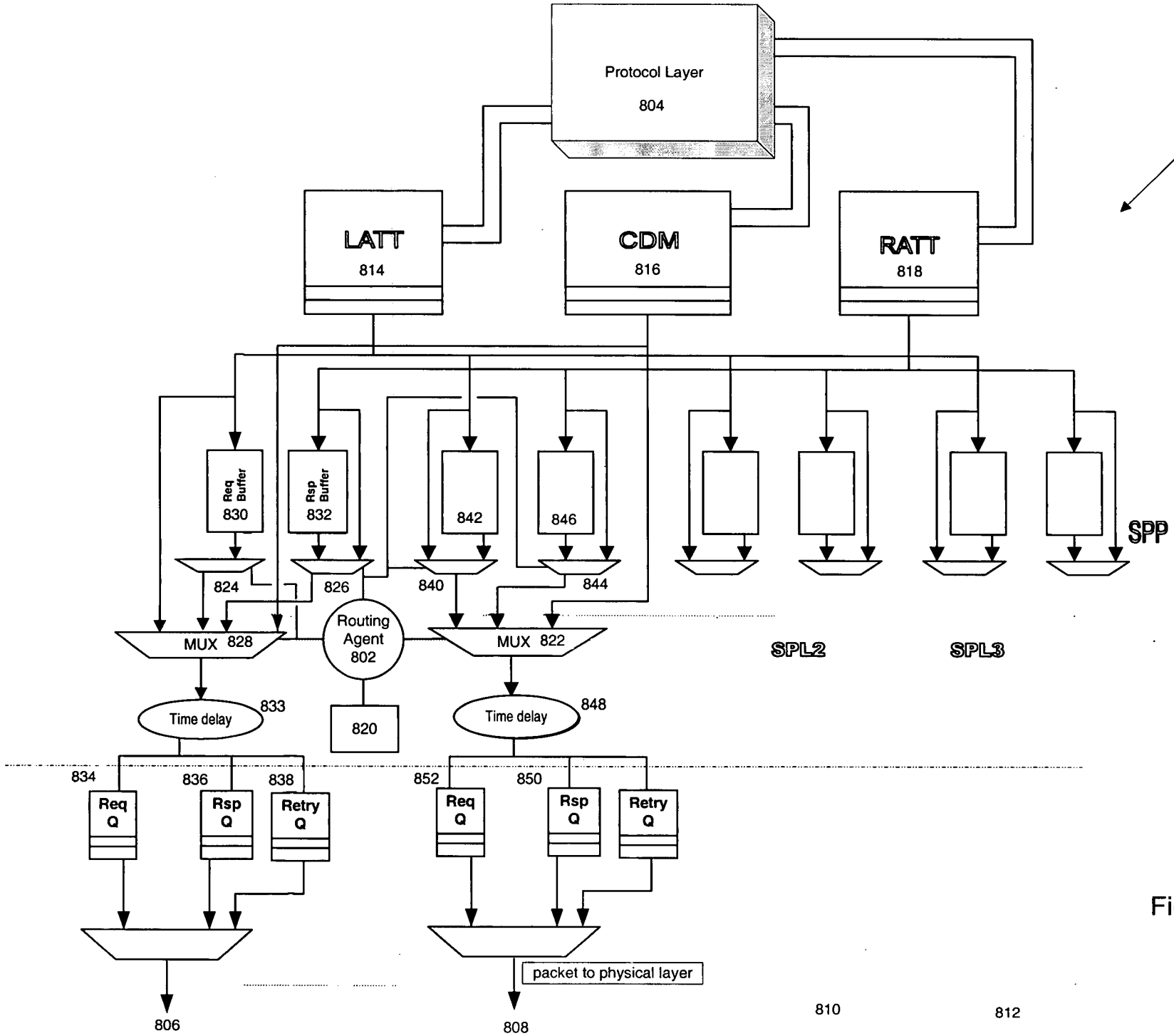

Figure 8

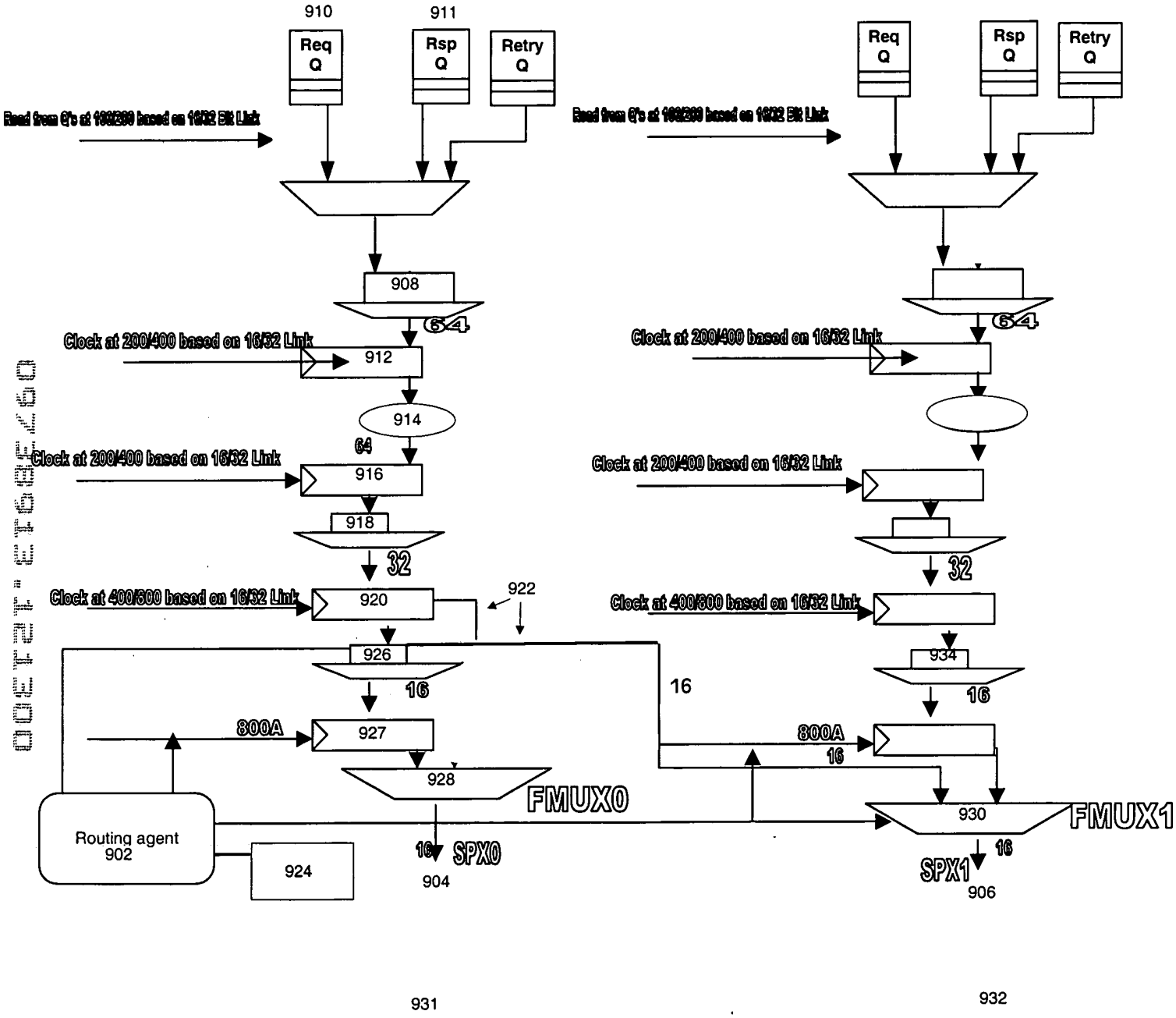
910
911
Req Q
Rsp Q
Retry Q
908
64
Clock at 200/400 based on 16/32 Link
912
914
64
916
Clock at 200/400 based on 16/32 Link
918
32
Clock at 400/300 based on 16/32 Link
920
922
926
16
800A
927
928
FMUX0
Routing agent 902
924
16
SPX0
904
931
Req Q
Rsp Q
Retry Q
64
Clock at 200/400 based on 16/32 Link
Clock at 200/400 based on 16/32 Link
32
Clock at 400/300 based on 16/32 Link
934
16
16
800A
16
930
FMUX1
16
SPX1
906
932
900

Figure 9